RECEIVED
CENTRAL FAX CENTER

OCT 25 2006

REMARKS

Claims 1-14 are presently pending in the application.

The Office Action has applied new grounds of rejection to claims 1-14. In particular, the Office Action has now rejected claims 1 and 2 under 35 U.S.C. § 102(b) as allegedly being anticipated by Clampitt et al. (U.S. Patent No. 6,414,351), rejected claim 3 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clampitt et al. in view of Hurley (U.S. Application Publication No. 2003/0013253), rejected claim 4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clampitt et al. in view of Hurley and further in view of Kokubu (U.S. Patent No. 6,200,858), rejected claims 5-7 and 10 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clampitt et al. in view of Hurley and further in view of Keller et al. (U.S. Patent No. 5,985,719), rejected claims 8 and 9 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clampitt et al. in view of Hurley and further in view of Keller et al. and further in view of Tay et al. (U.S. Application Publication No. 2002/0009900), rejected claims 11 and 12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clampitt et al. in view of Hurley and further in view of Keller et al. and Tay et al., and further in view of Ma et al. (U.S. Patent No. 6,207,586), and rejected claims 13 and 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Clampitt et al. in view of Gill (U.S. Patent No. 5,420,060). Applicants respectfully traverse these rejections.

In connection with these rejections, Applicants would like to thank Examiner Richard A. Booth for the Examiner Interview conducted with Applicants' representative, Kenton R. Mullins, on October 23, 2006. In this discussion, it was indicated by Examiner Booth that independent claim 1 would appear to distinguish over the prior art of record, assuming the Applicants' arguments' were technically correct, which they appeared to be. It was suggested that submission of the current Amendment by Applicants would appear to result in withdrawal of the outstanding prior-art rejections to the extent a closer review of the prior art of record does not lead to a new impression by the Examiner of the content of the prior art of record. Examiner Booth expressly reserved the right, however, to study and consider the matter further and to conduct an update search. Accordingly, as a result and for the reason of

the mentioned Examiner Interview, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 and § 103.

Concerning the Office Action's rejection of independent claim 1 under 35 U.S.C. § 102(b), it is well known that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Emphasis added; Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). Thus, for a rejection under 35 U.S.C. § 102(b) to be proper, every limitation recited in a claim, which is rejected as being anticipated by a prior-art reference, must be clearly disclosed in that single prior-art reference. In the instant case, Applicants respectfully submit that the cited Clampitt et al. reference does not disclose each and every element that is recited in the rejected claims as amended, and, therefore, the cited Clampitt et al. reference does not anticipate the claims under 35 U.S.C. § 102(b).

In the instant case, applying the above standard, the prior art references of record neither disclose, teach nor suggest any of Applicants' claimed combinations of processes for forming memory devices. More particularly, these prior art references, when considered alone or in combination, do not appear to teach or suggest, for example, Applicants' claimed combinations of a method for forming a memory device, including, among other things, "providing a stacked structure on a substrate, the stacked structure comprising a first dielectric, a floating gate, a second dielectric, and a control gate; forming a liner dielectric layer, which extends in a direction transverse to a bit line direction and substantially parallel to the control gate, on sidewalls of the stacked structure; and forming a barrier layer on at least part of the liner dielectric layer but not overlying source/drain regions of the memory device" (emphasis added), as recited in independent, amended claim 1.

With reference to Figure 8A of Clampitt et al., Applicants submit that the alleged barrier layer 173 of Clampitt et al. extends over the source/drain region of that memory device. Column 7, lines 3-8 of Clampitt et al. state that "[i]n one embodiment, N and P regions are formed in silicon substrate 110, and then the gate oxide layer(s) are grown. In other embodiments, self-aligned gates are formed by diffusing source and drain regions using

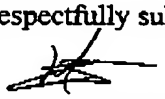
formed gate structures (described below) as masks." This language would inherently suggest, using the only reasonable interpretation, that the source/drain regions of Clampitt et al. extend all of the way to the borders of the Clampitt et al. gate structures, so that the alleged barrier layer 173 of Clampitt et al. would inherently, and necessarily, extend over the respective source/drain region. Furthermore, column 11, lines 43-45 of Clampitt et al. state that "[a] nitride spacer 172 is then deposited and etched, forming a spacer on the vertical sidewall over the source and drain ends of the floating-gate stacks," which again denotes that the source/drain regions extend to the border of the Clampitt et al. gate structures, so that the alleged barrier layer 173 of Clampitt et al. must extend over the respective source/drain region. Claim 1 of the Clampitt et al. reference provides further support for this disclosed architecture.

Now, regarding Applicants' presently claimed invention, in accordance with one aspect, a SiN barrier layer can be added onto a flash memory word-line sidewall to attenuate or prevent the so called "over-erase" issue. For flash memory structures such as described in Applicants' specification, higher electrical fields tend to exist at the four corners of a memory-cell channel during Fowler-Nordheim (F-N) erase operations. Thus, such operations tend to cause over-erase phenomena by way of electrons being more apt to tunnel out through these four corners. By adding a SiN barrier layer along the sidewall of the word line, the tunneling electrons at the mentioned corners can be captured by the SiN barrier layer, and the edge electrical field can be reduced to thereby effectively close the relatively easy tunneling paths. Thus, in accordance with an aspect of the present invention, a SiN barrier layer can be added on the word-line sidewall for enhanced operation of the resulting memory device. Furthermore, regarding the oxide layer, which is deposited before the SiN barrier layer, this oxide layer can in the context of the presently claimed invention improve flash memory reliability, since, for example, the SiN barrier layer material can undergo higher mechanical stress and the tunneling oxide can be damaged after SiN deposition and following thermal processes. This oxide layer can thus act as a stress release layer for the SiN barrier layer.

Accordingly, it is submitted that claim 1 distinguishes over the prior art of record. It is respectfully submitted that the presently pending dependent claims are allowable at least because of their dependencies upon independent, amended claim 1, and further because of the additional limitations recited in those dependent claims. Applicants, again, based upon the aforementioned reasons, respectfully request reconsideration and withdrawal of the rejections of the presently pending claims under 35 U.S.C. §§ 102(b) and 103(a).

In view of the above, Applicants submit that the application is now in condition for allowance, and an early indication of same is requested. Should the Examiner believe that a telephone conference with Applicants' representative would be helpful to advance the prosecution of the application, the Examiner is invited to contact the undersigned with any questions.

Respectfully submitted,



October 25, 2006

Kenton R. Mullins
Attorney for Applicants
Registration No. 36,331

STOUT, UXA, BUYAN & MULLINS, LLP
4 Venture, Suite 300
Irvine, CA 92618
Tel: 949-450-1750
Fax: 949-450-1764